Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 9-54.

Listing of Claims:

1. (Original) A clock signal generator having an input at which an input clock signal is applied and having an output at which an output clock signal is provided, the clock signal generator comprising:

a synchronizing circuit having an input terminal at which the input clock signal is applied and having an output terminal at which a first clock signal is provided, the synchronizing circuit generating the first clock signal based on the input clock signal; and

a plurality of delay circuits, each having an input coupled to the output terminal of the synchronizing circuit, and having an activation terminal at which a selection signal is applied and further having an output terminal at which a respective delayed output clock signal is provided, each of the plurality of delay circuits having a respective time delay and operable to generate the respective delayed output clock signal having the respective time delay relative to the first clock signal when activated by the selection signal, one of the plurality of delay circuits activated by the selection signal to provide the respective delayed output clock signal as the output clock signal of the clock signal generator.

2. (Original) The clock signal generator of claim 1 wherein the synchronizing circuit comprises a delay-locked loop (DLL).

3. (Original) The clock signal generator of claim 2 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency.

4. (Original) The clock signal generator of claim 3 wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time

delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

5. (Original) The clock signal generator of claim 1 wherein each of the plurality of delay circuits comprises a programmable delay element.

6. (Original) The clock signal generator of claim 5 wherein each of the programmable delay elements comprise a delay element programmable by programming antifuses.

7. (Original) The clock signal generator of claim 1 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value.

8. (Original) The clock signal generator of claim 7 wherein the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

9-54. (Cancelled)